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IMPLEMENTATION OF FLOATING POINT MULTIPLIER USING VHDL

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ABSTRACT

In this paper, multiplication of the floating point numbers described in IEEE 754 single precision valid. Floating point multiplier is done using VHDL .Implementation in VHDL(VHSIC Hardware Description Language) is used because it allow direct implementation on the hardware while in other language we have to convert them into HDL then only can be implemented on the hardware. In floating point multiplication, adding of the two numbers is done with the help of various types of adders but for multiplication some extra shifting is needed.This floating point multiplication handles various conditions like overflow, underflow, normalization, rounding. In this paper we use IEEE rounding method for perform the rounding of the resulted number.This paper reviews the implementation of an IEEE 754 single precision floating point multiplier developed by many researchers.

KEYWORDS: Floating Point Unit, XILINX ISE 8.1E as Synthesizer, MODEL-SIM as Simulator, Floating Point Arithmetic, Booth Multiplier, IEEE Rounding Method, Serial by Parallel Adder